REMARKS

Summary of the Office Action

Claims 1, 5 and 55-58 are considered in the Office action.

Claims 1, 5 and 57 have been rejected under 35 U.S.C. § 102(b) as anticipated by Steinmetz, Jr. U.S. Patent No. 5,600,579 ("Steinmetz").

Claims 55, 56 and 58 have been rejected under 35 U.S.C. § 103(a) as obvious over Steinmetz in view of Hansen Dai et al., "Multithreading VHDL Simulation," pp. 4.33-4.38, 1994 ("Dai").

Summary of the Reply

Applicants have amended claim 1 to more particularly point out and distinctly claim the invention, and have cancelled claims 55, 56 and 58 without prejudice.

Reply to Rejections Under 35 U.S.C. § 102(b)

Claims 1, 5 and 57 have been rejected under § 102(b) as anticipated by Steinmetz. Amended claim 1 recites a method for providing a design test bench, the method including providing a single executable program that partitions functionality of the test bench between a simulation engine and one or more scripted routines. Support for the amended claim language may be found in the specification at least at page 2, lines 31-32 ("This library [of PLI routines] allows multiple Tcl interpreters to be instantiated in VERILOG test benches.") (emphasis added); page 4, lines 32-34 ("the Tcl server runs on a separate thread from the VERILOG simulation.") (emphasis added); page 5, lines 8-9 ("The TCL_PLI library allows any number of Tcl interpreters to be instantiated in a VERILOG simulation.") (emphasis added); and page 5, lines 16-18 ("PLI routines are also provided that allow direct sharing of information between Tcl and VERILOG . . . .") (emphasis added) (all references to substitute specification filed on 25 April 2005). Indeed, applicants respectfully submit that a person of ordinary skill in the art would understand from reading the entire specification, and particularly the above-cited portions of the specification, that the claimed method provides a single executable program that partitions functionality of a test bench between a simulation

engine (i.e., the VERILOG simulator) and one or more scripted routines (i.e., the Tcl routines run by the Tcl interpreters).

Steinmetz does not describe or suggest the claimed invention, and in fact, distinctly points away from the claimed invention. In particular, Steinmetz describes a hardware design verification system including simulator means, test script means and dispatch means, each of which is a separate executing computer program under control of an operating system that provides for concurrent execution of computer programs. (Col. 3, lines 3-6; Col. 3, lines 20-24). Hardware design verification system 100 includes a number of program modules that execute concurrently on a time-sharing operating system. (Col. 4, line 66 through Col. 5, line 3). The program modules include simulation environment 101, test script 103 and dispatch module 105. (Col. 5, lines 21-22; Col. 5, lines 36-37; Col. 5, lines 47-48). Simulation environment 101 provides the resources for modeling the operation of circuit under test 115 and master model 113. (Col. 5, lines 22-27). Test script 103 is designed to test particular features of circuit under test 115. (Col. 5, lines 37-38). Dispatch module 105 bridges the executing test script 103 and simulation environment 101 by forking off the test script and the simulation environment as child processes that run independently of the dispatch means, which is the parent process. (Col. 3, lines 26-29; Col. 5, lines 47-51). Dispatch module 105 communicates with simulation environment and with test script 103 via data socket-based packet communication. (Col. 56-59).

Unlike the claimed invention, Steinmetz does not describe or suggest providing a single executable program that partitions functionality of a test bench between a simulation engine and one or more scripted routines. Indeed, Steinmetz' system uses separate executable programs to implement simulation environment 101, test script 103 and dispatch module 105. This distinction is significant, because the claimed methods offer several advantages over the Steinmetz approach. Indeed, the claimed methods allow faster communication between the simulation engine and the scripted routines than Steinmetz' socket-based communication approach. As a result, the claimed methods require less overhead than the Steinmetz system, in which communication between test scripts 103 and simulation environment 101 occurs only via sockets.

Because Steinmetz does not describe or suggest the claimed invention, applicants respectfully request that the §102(b) rejection of claim 1 be withdrawn. Because claims 5 and 57 depend from claim 1, applicants further respectfully request that the §102(b) rejection of claims 5 and 57 be withdrawn.

Reply to Rejections Under 35 U.S.C. § 103(a)

Applicants have cancelled claims 55, 56 and 58 without prejudice. Accordingly, applicants respectfully submit that the § 103 rejections are moot.

Conclusion

For the reasons stated above, applicants submit that this application, including claims 1, 5 and 57, is allowable. Applicants therefore respectfully request that the Examiner allow this application.

Respectfully submitted,

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